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May 24, 2000

ATTN: BOX PCT
Assistant Commissioner for Patents
Washington, D.C. 20231

ATTN: BOX PCT

Re: Application of **Dong-kyu KIM, Sang-hyun DO and Hyung-jin CHOI**
ORTHOGONAL FREQUENCY DIVISION MULTIPLEXING RECEIVER WHERE FFT WINDOW POSITION RECOVERY INTERLOCKS WITH SAMPLING CLOCK ADJUSTMENT AND METHOD THEREOF
Our Reference: Q58827
PCT/KR98/00376, filed November 24, 1998

Dear Sir:

Applicants herewith submit the attached papers for the purpose of entering the National stage under 35 U.S.C. § 371 and in accordance with Chapter II of the Patent Cooperation Treaty. Attached hereto is the application identified above which is a translation of **PCT International Application No. PCT/KR98/00376, filed November 24, 1998**, comprising the specification, claims, drawings and International Search Report. **The executed Declaration and Power of Attorney and Assignment will be submitted at a later date.**

The Government filing fee is calculated as follows:

Total Claims	7 - 20 =	0 x $18 =	$ 000.00
Independent Claims	2 - 3 =	0 x $78 =	$ 000.00
Base Filing Fee	($970.00)		$ 970.00
Multiple Dep. Claim Fee	($260.00)		$ 000.00
TOTAL FILING FEE			**$ 970.00**

A check for the statutory filing fee of $ **970.00** is attached. You are also directed and authorized to charge or credit any difference or overpayment to Deposit Account No. 19-4880. The Commissioner is hereby authorized to charge any fees under 37 C.F.R. 1.492; 1.16 and 1.17 and any petitions for extension of time under 37 C.F.R. 1.136 which may be required during the entire pendency of the application to Deposit Account No. 19-4880. A duplicate copy of this transmittal letter is attached.

Priority is claimed from:

Korean Patent Application	Filing Date
97-62690	November 25, 1997

Respectfully submitted,
SUGHRUE, MION, ZINN, MACPEAK & SEAS
Attorneys for Applicant(s)

By: _____
Darryl Mexic
Reg. No. 23,063

DM:amt

PATENT APPLICATION
Q58827

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Dong-ku KIM, Sang-hyun DO and Hyung CHOI

Application No: 09/555,046 Group Art Unit: UNKNOWN

Filed: May 24, 2000 Examiner: UNKNOWN

For: ORTHOGONAL FREQUENCY DIVISION MULTIPLEXING RECEIVER WHERE FFT WINDOW POSITION RECOVERY INTERLOCKS WITH SAMPLING CLOCK ADJUSTMENT AND METHOD THEREOF

PRELIMINARY AMENDMENT

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

Please enter the following amendments to the application prior to examination:

IN THE SPECIFICATION:

Page 5, line 3, delete "216" and insert --218--.

line 4, delete "216" and insert --218--.

Page 5, line 12, delete "$\gamma(\bullet)$" and insert -- $\gamma[\hat{\tau}_1]$ --

IN THE CLAIMS:

1. (Amended) A method of interlocking FFT window position recovery with sampling clock control in symbol units in an orthogonal frequency division multiplexing (OFDM) receiver for receiving an OFDM symbol consisting of a useful data interval and a guard interval, the method comprising the steps of:

(a) extracting a pilot signal from fast-Fourier-transformed OFDM received signals, and detecting inter-pilot phase differences;

(b) averaging phase differences detected in step (a) for a symbol to generate a mean phase difference value and normalizing the mean phase difference by dividing [it] the mean

phase difference value into reference values corresponding to phase differences generated when FFT window errors of at least one sample exist, thereby to generate a normalized value; and

(c) simultaneously controlling the FFT window position offset using a value obtained by rounding off the normalized value of the step (b), and the sampling clock offset using the difference between the round-off value and the normalized value.

3. (Amended) An OFDM receiver for interlocking FFT window position recovery with sampling clock control by receiving an OFDM symbol consisting of a useful data interval and a guard interval, the apparatus comprising:

an analog-to-digital converter (ADC) for converting an OFDM signal into digital complex samples;

an FFT window for removing the guard interval from the digital complex samples output by the ADC and outputting useful data samples;

an FFT for fast-Fourier-transforming the samples output by the FFT window;

a phase difference calculator for calculating phase differences between two values among the complex values received via a plurality of pilots from the FFT, averaging [these] the phase differences for one symbol to generate a mean phase difference value, and normalizing the mean phase difference value by dividing [it] the mean phase difference value into predetermined reference values;

an FFT window controller for rounding off the normalized value output by the phase difference calculator and controlling the window position of the FFT window; and

a phase synchronous loop for controlling the sampling clock signals of the ADC using the difference between the round-off value and the normalized value.

4. (Amended) The OFDM receiver for interlocking FFT window position recovery with sampling clock control as claimed in claim 3, wherein the phase difference calculator comprises:

a phase difference detector for detecting the phase differences between two pilots among the received complex values of the pilots output by the FFT;

a mean calculator for averaging the phase differences detected by the phase detector for [a] one symbol and generating the mean phase difference value; and

a normalizer for normalizing the mean value obtained by the mean calculator by dividing [it] the mean phase difference value into reference values corresponding to phase differences generated when an FFT window error of one sample exists.

7. (Amended) The OFDM receiver for interlocking FFT window position recovery with sampling clock control as claimed in claim 4, wherein the normalization of the normalizer is carried out by multiplying $\frac{N}{2\pi}$ [to] by the mean value.

REMARKS

General remarks:

Claims 1-7 are all the claims pending in the application. The specification is amended to correct noted informalities. Claims 1, 3, 4, and 7 are amended for clarity and to correct informalities. Applicant respectfully requests the Examiner to enter this Amendment prior to examining the application.

Applicant hereby petitions for any extension of time which may be required to maintain the pendency of this case, and any required fee, except for the Issue Fee, is to be charged to Deposit Account No. 19-4880.

Respectfully submitted,

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Date: August 11, 2000

ORTHOGONAL FREQUENCY DIVISION MULTIPLEXING RECEIVER WHERE FFT WINDOW POSITION RECOVERY INTERLOCKS WITH SAMPLING CLOCK ADJUSTMENT AND METHOD THEREOF

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an orthogonal frequency division multiplexing (OFDM) receiver and a method thereof, and more particularly, to an OFDM receiver for interlocking FFT window position recovery with sampling clock control for controlling an analog-to-digital converter, and a method thereof.

2. Description of the Related Art

Generally, time synchronization and frequency synchronization must be accurately performed to allow a receiver to recover an OFDM signal for European digital broadcasts transmitted from a transmitter. Time synchronization consists of FFT window position recovery for accurate parallel processing of signals, and sampling clock recovery for controlling a sampling clock of an analog-to-digital converter (ADC) for sampling a signal having a maximum signal-to-noise ratio (SNR) among received signals. Frequency synchronization means that the radio frequency (RF) oscillation frequency of a receiver is synchronized with the oscillation frequency of a transmitter.

FIG. 1 is a block diagram of a portion for carrying out FFT window position recovery and sampling clock control in a general OFDM system receiver.

When the number of bins of FFT is N, the symbol of an OFDM signal is comprised of a useful data interval having N useful data samples being the outputs of an inverse fast Fourier transform (IFFT), and a guard interval having G sample lengths to be inserted between symbols to prevent inter-symbol interference. The guard interval copies the end portion of the useful data interval. A transmitter (not shown) sequentially transmits a symbol consisting of G+N samples being the sum of N complex values and G complex values output by the IFFT.

An i-th symbol comprised of complex values output by an FFT is expressed by the following Equation 1:

$$s_l = \sum_{n=-G}^{N-1} x_{l,n} = \sum_{n=-G}^{-1} \sum_{k=0}^{N-1} X_{l,k} e^{j2\pi(N+n)l/N} + \sum_{n=0}^{N-1} \sum_{k=0}^{N-1} X_{l,k} e^{j2\pi kn/N} \quad \text{...(1)}$$

wherein l is a symbol number, k is a carrier index (number), N is the number of useful data samples, and n represents sampling time. The first term of the second expression of Equation 1 represents a guard interval, and the second term represents a useful data interval.

As shown in FIG. 1, an ADC 110 samples a received OFDM signal. An FFT window 120 is controlled by an FFT window controller 180 to recover an FFT window position, and removes the guard interval of the first term of Equation 1 and then sequentially transmits the second term to the FFT 130. A phase difference calculator 150 calculates a phase difference between two pilots extracted by a pilot extractor 140 for one symbol. An FFT window offset detector 160 detects the position of the FFT window by the phase difference output by the phase difference calculator 150. The FFT window controller 180 controls the position of the FFT window by the FFT window offset. When FFT window position recovery is not carried out well, the received signal cannot be accurately recovered since sampling clock control is also not carried out well. Hence, the sampling clock control starts after FFT window position recovery by the FFT window controller 180 is completed. In other words, the phase difference calculator 150 calculates phase differences between pilots extracted between current and previous symbols by the pilot extractor 140 after the FFT window position recovery is completed. A sampling clock offset detector 170 detects sampling offsets using the phase difference output by the phase difference calculator 150. A phase-locked loop (PLL) 190 controls the sampling clocks of the ADC 110 according to input sampling clock offsets. If the sampling clocks are not controlled, the receiver is not sampled into a total of (N+G) samples for one symbol but sampled into (N+G+1) or (N+G-1) samples because of a sampling clock difference between the receiver and transmitter, resulting in a sample stuff-rob phenomenon. As a consequence, a next symbol start point is preceded or delayed by one sample. Therefore, the apparatus of FIG. 1 controls

sampling clock errors after accurate FFT window position recovery is carried out, and thus the sample stuff-rob phenomenon is generated while FFT position recovery is performed.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide an OFDM receiver for simultaneously carrying out FFT window position recovery and sampling clock control using a detected phase difference between two pilots in one symbol period, and a method thereof.

To accomplish the above object, there is provided a method of interlocking FFT window position recovery with sampling clock control in symbol units in an orthogonal frequency division multiplexing (OFDM) receiver for receiving an OFDM symbol consisting of a useful data interval and a guard interval, the method including the steps of: (a) extracting a pilot signal from fast-Fourier-transformed OFDM received signals, and detecting inter-pilot phase differences; (b) averaging phase differences detected in step (a) for a symbol and normalizing the mean phase difference by dividing it into reference values corresponding to phase differences generated when FFT window errors of at least one sample exist; and (c) simultaneously controlling the FFT window position offset using a value obtained by rounding off the normalized value of the step (b), and the sampling clock offset using the difference between the round-off value and the normalized value.

To accomplish the above object, there is provided an OFDM receiver for interlocking FFT window position recovery with sampling clock control by receiving an OFDM symbol consisting of a useful data interval and a guard interval, the apparatus including: an analog-to-digital converter (ADC) for converting an OFDM signal into digital complex samples; an FFT window for removing the guard interval from the digital complex samples output by the ADC and outputting useful data samples; an FFT for fast-Fourier-transforming the samples output by the FFT window; a phase difference calculator for calculating phase differences between two values among the complex values received via a plurality of pilots from the FFT, averaging these phase differences for one symbol, and normalizing the mean value by dividing it into predetermined reference values; an FFT window controller for

rounding off the normalized value output by the phase difference calculator and controlling the window position of the FFT window; and a phase synchronous loop for controlling the sampling clock signals of the ADC using the difference between the round-off value and the normalized value.

BRIEF DESCRIPTION OF THE DRAWINGS

The above object and advantage of the present invention will become more apparent by describing in detail a preferred embodiment thereof with reference to the attached drawings in which:

FIG. 1 is a block diagram showing the configuration of a general OFDM system receiver;

FIG. 2 is a block diagram of an OFDM receiver for interlocking FFT window position recovery with sampling clock control, according to the present invention;

FIG. 3 is a conceptual view showing the division of time synchronization into an FFT window offset and a sampling clock offset by using the round-off calculator 224 and the subtractor 226 of FIG. 2;

FIG. 4A is a graph showing outputs of the phase difference calculator vs. FFT window offsets, according to the present invention;

FIG. 4B is a graph showing inputs of the FFT window controller vs. FFT window offsets, according to the present invention; and

FIG. 4C is a graph showing inputs of the PLL for controlling sampling clock signals vs. FFT window offsets, according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. 2, an ADC 210 converts a received OFDM signal into a digital complex sample. An FFT window 212 removes a guard interval from the input digital complex sample and then sequentially outputs N sample values to an FFT 214. The FFT 214 fast-Fourier-transforms the input N sample values.

A pilot extractor 216 extracts complex values transmitted via pilots, among the outputs of the FFT 214. The pilots are specific subcarriers that are used when a transmitter transmits known values for synchronization of the receiver and transmitter in an OFDM system. In general, the OFDM system receiver is used for

synchronization by using the complex values transmitted via the pilots among the outputs of the FFT.

A phase calculator 240 includes a phase difference detector 216, a mean calculator 220, and a normalizer 222. The phase difference detector 216 detects a phase difference between a pair of pilots for one symbol. The mean calculator 220 averages the phase differences with respect to a plurality of pilot pairs. The normalizer 222 normalizes the mean value by dividing it into reference values corresponding to the volumes of phase changes occurring when an FFT window error of one sample exists. A normalized phase variation $\hat{\tau}_l$ calculated by the phase calculator 240 is expressed by the following Equation 2:

$$\hat{\tau}_l = \frac{\frac{1}{2\pi}}{N} \frac{1}{L} \sum_{n=1}^{l} \frac{\Delta\phi_{l,k_{n+1,n}}}{k_{n+1} - k_n} \quad \text{...(2)}$$

wherein N is the number of useful data samples, L is the number of used pilots, k is a subcarrier number, $k_{n+1}-k_n$ is a frequency spacing between two pilot carriers, and $\Delta\phi_{l,k_{n+1,n}}$ is a phase difference between pilots for a l-th symbol.

The phase calculator 240 will now be described in more detail. The phase difference detector 218 detects a phase difference between the pilot pair extracted by the pilot extractor 216. Phase difference detection changes according to the method of allocating known complex values between the transmitter and receiver transmitted via pilots. The phase difference detector according to a first method comprises a phase detector (not shown) for detecting the phases of input complex values when an identical complex value is allocated to each pilot independently of symbols and pilots, and a subtractor (not shown) for obtaining the difference between the phases calculated from the received complex values of two pilots. The phase difference detector according to a second method comprises a phase detector (not shown) for detecting the phase difference between an input complex value and a known complex value when different complex values are allocated for different pilots, and a subtractor (not shown) for obtaining the difference between the phases calculated from the received complex values of two pilots.

The mean calculator 220 averages a plurality of pilot pairs of the phase differences output by the phase difference detector 240 for an l-th symbol period.

A general OFDM system uses a plurality of pilots, and can obtain a more reliable value by averaging the pilots.

The normalizer 222 normalizes the mean calculated by the mean calculator 220 by dividing it into reference values. The reference value is set to be the magnitude of a phase change (N/2π) generated between two pilots when an FFT window offset is one sample.

The normalized phase variation output by the normalizer 222 is divided into an integer part and a fraction part by a round-off calculator 224 and a subtractor 226, and expressed by the following Equation 3:

$$\hat{\tau}_l = \gamma[\hat{\tau}_l] + \{\hat{\tau}_l - \gamma[\hat{\tau}_l]\} = (\textit{integer part}) + (\textit{fraction part}) \quad \textbf{...(3)}$$

wherein $\gamma(\bullet)$ is a round-off function, and the fraction part is between ±0.5.

FIG. 3 is a conceptual view showing a division of time synchronization into an FFT window offset and a sampling clock offset by using the integer part and fraction part.

As shown in FIG. 3, the slope of a phase variation is affected by both the FFT window offset and the sampling clock offset. That is, when the FFT window offset is one sample, the slope of an actual phase variation is changed for each symbol on the axis of the slope of a phase variation with respect to an FFT window offset of one sample within an FFT window offset decision area.

The FFT window 212 is controlled by an integer value output by the round-off calculator 224 because the FFT window offset is estimated in sample units.

The FFT window controller 228 receives the integer value output by the round-off calculator 224 and corrects FFT window position recovery errors of the FFT window 120.

The sampling clock offset of the ADC 210 is controlled to be within ±0.5. The PLL 230 receives a fraction value output by the subtractor 226 and controls the sampling clock offset of the ADC 210.

Consequently, the phase variation value output by the normalizer 222 simultaneously controls the FFT window via the round-off calculator 224 and the FFT window controller 228 and the sampling clock of the ADC 210 via the subtractor 226 and the PLL 230.

FIG. 4A is a graph showing outputs of the phase difference calculator 240 vs. FFT window offsets, according to the present invention. FIG. 4A shows normalized mean phase differences between two pilots output by the normalizer 222 when the FFT window offset is within ±5 samples.

FIG. 4B is a graph showing inputs of the FFT window controller 228 vs. FFT window offsets, according to the present invention. FIG. 4B shows values of FIG. 4A which have passed through the round-off calculator 224, and accurately predicts FFT window errors with respect to the FFT window offsets.

FIG. 4C is a graph showing inputs of the PLL 230 for controlling sampling clock signals vs. FFT window offsets, according to the present invention. FIG. 4C shows the difference between the input and output values of the round-off calculator 224 output by the subtractor 226, representing an accurate characteristics curve which is not affected by the FFT window offset when the FFT window offset is within ±5 samples.

Although the invention has been described with reference to a particular embodiment, it will be apparent to one of ordinary skill in the art that modifications of the described embodiment may be made without departing from the spirit and scope of the invention.

According to the present invention as described above, FFT window position recovery is carried out without being affected by sampling clock errors, and simultaneously sampling clocks are controlled without being affected by FFT window position recovery errors. Therefore, causes of an unstable system are removed, and a synchronization time can be shortened by the simultaneous operations of the two functions.

What is claimed is:

1. A method of interlocking FFT window position recovery with sampling clock control in symbol units in an orthogonal frequency division multiplexing (OFDM) receiver for receiving an OFDM symbol consisting of a useful data interval and a guard interval, the method comprising the steps of:

(a) extracting a pilot signal from fast-Fourier-transformed OFDM received signals, and detecting inter-pilot phase differences;

(b) averaging phase differences detected in step (a) for a symbol and normalizing the mean phase difference by dividing it into reference values corresponding to phase differences generated when FFT window errors of at least one sample exist; and

(c) simultaneously controlling the FFT window position offset using a value obtained by rounding off the normalized value of the step (b), and the sampling clock offset using the difference between the round-off value and the normalized value.

2. The method of interlocking FFT window position recovery with sampling clock control in an OFDM receiver as claimed in claim 1, wherein the FFT window position offsets are controlled by integer values, and the sampling clock offsets are controlled by fraction values.

3. An OFDM receiver for interlocking FFT window position recovery with sampling clock control by receiving an OFDM symbol consisting of a useful data interval and a guard interval, the apparatus comprising:

an analog-to-digital converter (ADC) for converting an OFDM signal into digital complex samples;

an FFT window for removing the guard interval from the digital complex samples output by the ADC and outputting useful data samples;

an FFT for fast-Fourier-transforming the samples output by the FFT window;

a phase difference calculator for calculating phase differences between two values among the complex values received via a plurality of pilots from the FFT,

averaging these phase differences for one symbol, and normalizing the mean value by dividing it into predetermined reference values;

an FFT window controller for rounding off the normalized value output by the phase difference calculator and controlling the window position of the FFT window; and

a phase synchronous loop for controlling the sampling clock signals of the ADC using the difference between the round-off value and the normalized value.

4. The OFDM receiver for interlocking FFT window position recovery with sampling clock control as claimed in claim 3, wherein the phase difference calculator comprises:

a phase difference detector for detecting the phase differences between two pilots among the received complex values of pilots output by the FFT;

a mean calculator for averaging the phase differences detected by the phase detector for a symbol; and

a normalizer for normalizing the mean value obtained by the mean calculator by dividing it into reference values corresponding to phase differences generated when an FFT window error of one sample exists.

5. The OFDM receiver for interlocking FFT window position recovery with sampling clock control as claimed in claim 4, wherein the phase difference of the phase difference detector is set to be $\frac{\Delta\Phi_{i,k_{n+1},n}}{k_{n+1}-k_n}$, $k_{n+1}-k_n$ is a frequency spacing between two pilot carriers, and $\Delta\Phi_{i,k_{n-1},n}$ is an inter-pilot phase difference for an i-th symbol.

6. The OFDM receiver for interlocking FFT window position recovery with sampling clock control as claimed in claim 4, wherein the mean value of the mean calculator is set to be $\frac{1}{L}\sum_{n=1}^{L}\frac{\Delta\Phi_{i,k_{n+1},n}}{k_{n+1}-k_n}$, and L represents the number of used pilots.

7. The OFDM receiver for interlocking FFT window position recovery with sampling clock control as claimed in claim 4, wherein the normalization of the normalizer is carried out by multiplying $\frac{N}{2\pi}$ to the mean value.

Abstract of the Disclosure

An OFDM receiver for interlocking FFT window position recovery with sampling clock control, and a method thereof are provided. This method includes the steps of: extracting a pilot signal from fast-Fourier-transformed OFDM received signals, and detecting inter-pilot phase differences; averaging the detected phase differences for a symbol and normalizing the mean phase difference by dividing it into reference values corresponding to phase differences generated when FFT window errors of at least one sample exist; and simultaneously controlling the FFT window position offset using a value obtained by rounding off the normalized value, and the sampling clock offset using the difference between the round-off value and the normalized value.

FIG. 1

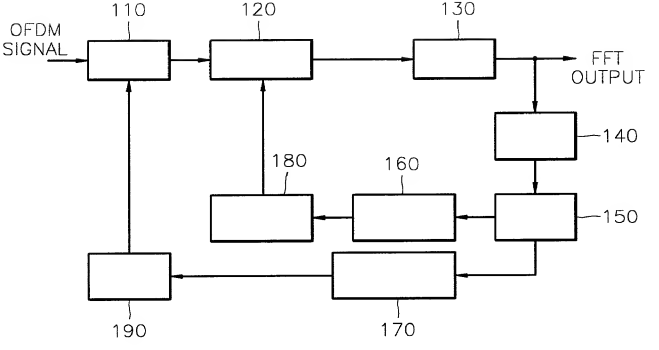

OFDM SIGNAL
110
120
130
FFT OUTPUT
140
180
160
150
190
170

FIG. 2

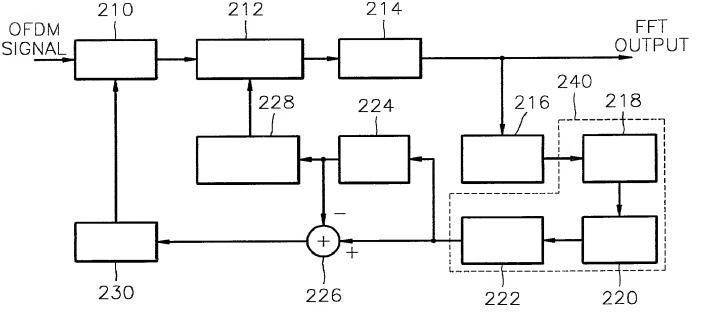

OFDM SIGNAL
210
212
214
FFT OUTPUT
240
228
224
216
218
230
226
222
220

FIG. 3

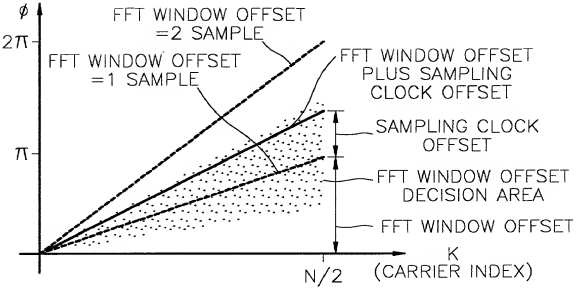


FIG. 4A

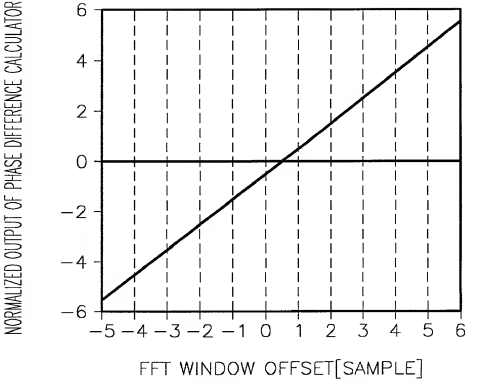

NORMALIZED OUTPUT OF PHASE DIFFERENCE CALCULATOR
6
4
2
0
−2
−4
−6
−5 −4 −3 −2 −1 0 1 2 3 4 5 6
FFT WINDOW OFFSET[SAMPLE]

FIG. 4B

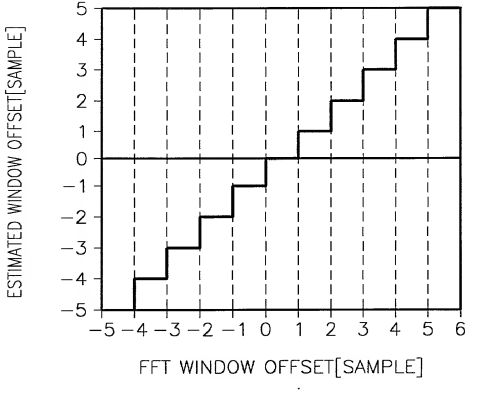
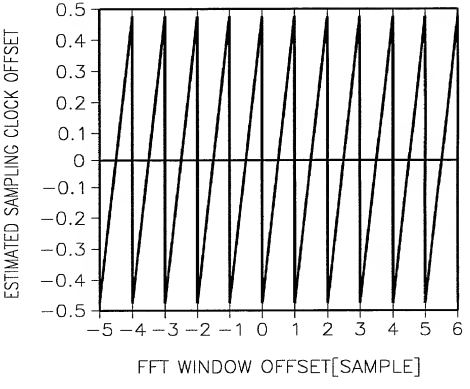

ESTIMATED WINDOW OFFSET[SAMPLE]
5
4
3
2
1
0
−1
−2
−3
−4
−5
−5 −4 −3 −2 −1 0 1 2 3 4 5 6
FFT WINDOW OFFSET[SAMPLE]

FIG. 4C



Declaration and Power of Attorney For Patent Application
출원서원본상의 선서서와 위임장

Korean Language Declaration
한국어 선서서

하기한 발명자인 본인은 다음과 같이 선서합니다:

As a below named inventor, I hereby declare that:

본인의 주소, 우편주소 및 국적은 본인의 이름밑에 기재된 바와 같습니다.

My residence, post office address and citizenship are as stated next to my name.

본인은 아래에 기재된 발명에 대한 최초의 단독발명자 (단 한사람의 이름이 아래에 기재되었을 경우) 또는 공동발명자 (복수의 발명자가 아래에 기재되었을 경우) 라고 믿습니다.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

ORTHOGONAL FREQUENCY DIVISION MULTIPLEXING RECEIVER WHERE FFT WINDOW POSITION RECOVERY INTERLOCKS WITH SAMPLING CLOCK ADJUSTMENT AND METHOD THEREOF

아래 박스에 표시가 되어있지 않는 한 특허설명서는 여기에 첨부되어 있음:

the specification of which is attached hereto unless the following box is checked:

☐ __월 __일 미국출원번호 또는 PCT국제출원번호 _____로 출원되었으며 __ 월 __일 수정되었습니다. (만약 적용가능하면)

☒ was filed on 24 May 2000 as United States Application Number or PCT International Application Number 09/555,046 and was amended on _____ (if Applicable). 24/November/1998 PCT/KR 98/00376

본인은 상기 수정출원을 포함하여 특허설명서 내용을 검토하였으며 잘 파악하고 있음을 선서합니다.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

본인은 연방규정법전 37장 1.56편에 따라 특허자격에 있어 중요한 정보자료를 밝히는 것이 본인의 의무임을 인정합니다.

I acknowledge the duty to disclose information which is material to patentability as defined in the Title 37, Code of Federal Regulations, Section 1.56.

Korean Language Declaration
한국어 선서서

본인은 미합중국법전 35장 119(a)-(d)편 또는 특허 또는 발명자 증서를 위한 그 어떤 외국출원의 365(b)편 또는 미국 이외에 최소한 한 국가를 지정하는 PCT국제출원의 365(a)편하의 외국우선권을 주장합니다. 아래 박스에 표시함으로서 기재하고 확인합니다.

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

이전의 외국 출원

Priority Not Claimed
우선권 주장안함

(Number) (번호)	(Country) (국명)	(Day/Month/Year Filed) (출원년월일)	
97-62690	Rep. of Korea	25/November/1997	☐
			☐
			☐

본인은 미합중국법전 35장, 아래에 기재한 그 어떤 미국 가출원의 119(e)편하의 권한을 주장합니다.

I hereby claim the benefit under Title 35, United States Code, Section119(e) of any United States provisional application(s) listed below.

(Application No.) (출원번호)	(Filing Date) (출원일)	(Application No.) (출원번호)	(Filing Date) (출원일)

본인은 미합중국법전 35장, 그 어떤 미국출원의 120편 또는 미국을 지정하는 그 어떤 PCT국제출원의 365(c)편하의 권한을 주장합니다. 미합중국법전 35장 112편의 첫단락에 제시된 방법에 따라 이전의 미국 또는 PCT국제출원에 이제까지 기재된 본출원 내용은 밝혀지지 않았습니다. 본인은 연방규정법전 37장 1.56편에 따라 이전출원의 출원일과 국내 또는 PCT국제출원의 출원일사이에 유효된 특허자격에 있어 중요한 정보자료를 밝히는 것이 본인의 의무임을 인정합니다.

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112. I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No) (출원번호)	(Filing Date) (출원일)	(Status: Patented, Pending, Abandoned) (현황: 특허완료, 심사중, 포기됨)
(Application No.) (출원번호)	(Filing Date) (출원일)	(Status: Patented, Pending, Abandoned) (현황: 특허완료, 심사중, 포기됨)

본인이 아는 바에 의하면 여기에 작성된 모든 기재사항들과 정보자료로 제출한 모든 기재사항들은 진실된 것임을 선서하며, 그리고 이러한 진술이 고의적인 허위진술이거나 이와 비슷한 경우에는 미합중국법전 18장 1001편에 따라 벌금이나 징역형 또는 그 병과형으로 처벌되며, 허위진술은 본출원의 유효성이나 발급된 특허증을 위태롭게 할 수도 있다는 점을 선서합니다.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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위임장: 본인은 본건출원과 관련된 모든 사무를 처리하기 위하여 대리인을 지명합니다. 상기 각자는 대리와 치소 및 업무제휴가 되어있는 대리인을 지명할 전권을 갖습니다. (성명 및 등록번호 기재)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number)

I hereby appoint John H. Mion, Reg. No. 18,879; Donald E. Zinn, Reg. No. 19,046; Thomas J. Macpeak, Reg. No. 19,292; Robert J. Seas, Jr., Reg. No. 21,092; Darryl Mexic, Reg. No. 23,063; Robert V. Sloan, Reg. No. 22,775; Peter D. Olexy, Reg. No. 24,513; J. Frank Osha, Reg. No. 24,625; Waddell A. Biggart, Reg. No 24,861; Robert G. McMorrow, Reg. No. 19,093; Louis Gubinsky, Reg. No. 24,835; Neil B. Siegel, Reg. No. 25,200; David J. Cushing, Reg. No. 28,703; John R. Inge, Reg. No. 26,916; Joseph J. Ruch, Jr., Reg. No. 26,577; Sheldon I. Landsman, Reg. No. 25,430; Richard C. Turner, Reg. No. 29,710; Howard L. Bernstein, Reg. No. 25,665; Alan J. Kasper, Reg. No. 25,426; Kenneth J. Burchfiel, Reg No. 31,333; Gordon Kit, Reg. No. 30,764; Susan J. Mack, Reg. No. 30, 951; Frank L. Bernstein, Reg, No. 31,484; Mark Boland, Reg No. 32,197; William H. Mandir, Reg. No. 32,156; Scott M. Daniels, Reg. No. 32,562; Brian W. Hannon, Reg. No. 32,778; Abraham J. Rosner, Reg. No. 33,276; Bruce E. Kramer, Reg. No. 33,725; Paul F. Neils, Reg. No. 33,102; and Brett S. Sylvester, Reg, No. 32,765, my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and request that all correspondence about the application be addressed to SUGHRUE, MION, ZINN, MACPEAK & SEAS, PLLC. 2100 Pennsylvania Avenue, N.W., Washington, D.C. 20037-3202.

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(세번째와 그외 합동발명자의 위와 비슷한 기재사항과 서명을 제공하십시요.)

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